

## 2.5-V PHASE-LOCKED-LOOP CLOCK DRIVER

### FEATURES

- Spread-Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 220 MHz
- Low Jitter (Cycle-Cycle):  $\pm 60$  ps ( $\pm 40$  ps at 200 MHz)
- Low Static Phase Offset:  $\pm 50$  ps
- Low Jitter (Period):  $\pm 60$  ps ( $\pm 30$  ps at 200 MHz)
- 1-to-4 Differential Clock Distribution (SSTL2)
- Best in Class for  $V_{OX} = V_{DD}/2 \pm 0.1$  V
- Operates From Dual 2.6-V or 2.5-V Supplies
- Available in a 28-Pin TSSOP Package
- Consumes  $< 100$ - $\mu$ A Quiescent Current
- External Feedback Pins ( $\overline{\text{FBIN}}$ ,  $\overline{\text{FBIN}}$ ) Are Used to Synchronize the Outputs to the Input Clocks
- Meets/Exceeds JEDEC Standard (JESD82-1) For DDRI-200/266/333 Specification
- Meets/Exceeds Proposed DDRI-400 Specification (JESD82-1A)
- Enters Low-Power Mode When No CLK Input Signal Is Applied or  $\overline{\text{PWRDWN}}$  Is Low

### APPLICATIONS

- DDR Memory Modules (DDR400/333/266/200)
- Zero-Delay Fan-Out Buffer

### DESCRIPTION

The CDCVF855 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to 4 differential pairs of clock outputs ( $\overline{\text{Y}}[0:3]$ ,  $\overline{\text{Y}}[0:3]$ ) and one differential pair of feedback clock outputs ( $\overline{\text{FBOUT}}$ ,  $\overline{\text{FBOUT}}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks ( $\overline{\text{FBIN}}$ ,  $\overline{\text{FBIN}}$ ), and the analog power input ( $\text{AV}_{DD}$ ). When  $\overline{\text{PWRDWN}}$  is high, the outputs switch in phase and frequency with CLK. When  $\overline{\text{PWRDWN}}$  is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency-detection circuit detects the low-frequency condition and, after applying a  $>20$ -MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When  $\text{AV}_{DD}$  is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF855 is also able to track spread-spectrum clocking for reduced EMI.

Because the CDCVF855 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF855 is characterized for both commercial and industrial temperature ranges.

### AVAILABLE OPTIONS

$T_A$	TSSOP (PW)
$-40^\circ\text{C}$ to $85^\circ\text{C}$	CDCVF855PW

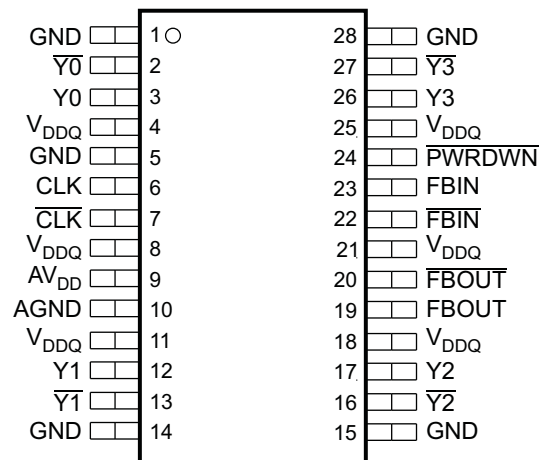


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE  
(Select Functions)**

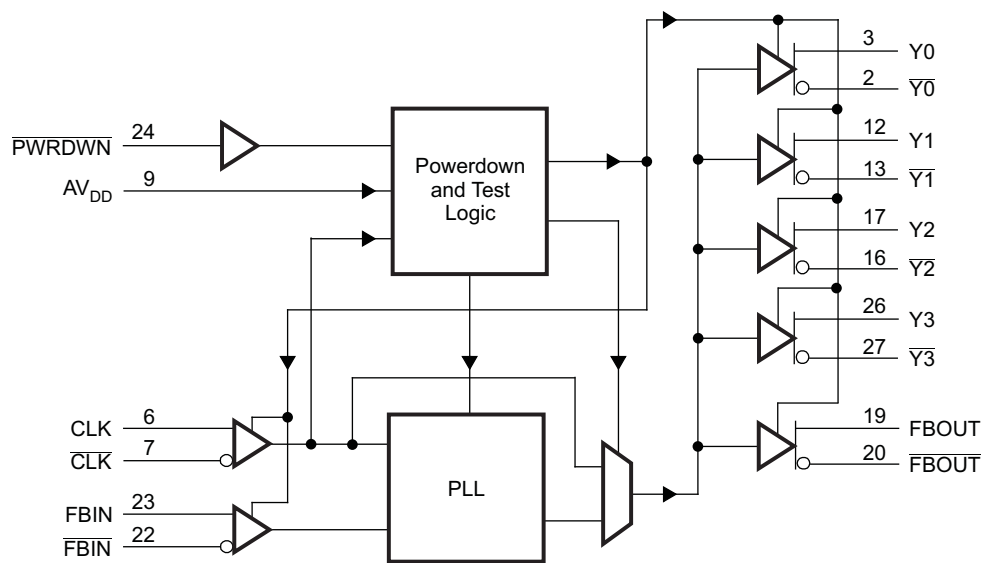
INPUTS				OUTPUTS				PLL
AVDD	PWRDWN	CLK	CLK	Y[0:3]	Y[0:3]	FBOUT	FBOUT	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

**PW PACKAGE  
(TOP VIEW)**



P0043-02

**FUNCTIONAL BLOCK DIAGRAM**



B0196-02

**Table 2. TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	10	–	Ground for 2.5-V analog supply
AV <sub>DD</sub>	9	–	2.5-V analog supply
CLK, $\overline{\text{CLK}}$	6, 7	I	Differential clock input
FBIN, FBIN	22, 23	I	Feedback differential clock input
FBOU, $\overline{\text{FBOU}}$	19, 20	O	Feedback differential clock output
GND	1, 5, 14, 15, 28	–	Ground
$\overline{\text{PWRDWN}}$	24	I	Output enable for Y and $\overline{\text{Y}}$
V <sub>DDQ</sub>	4, 8, 11, 18, 21, 25	–	2.5-V supply
$\overline{\text{Y0}}$ , Y0	2, 3	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$
Y1, $\overline{\text{Y1}}$	12, 13	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$
$\overline{\text{Y2}}$ , Y2	16, 17	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$
Y3, $\overline{\text{Y3}}$	26, 27	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

V <sub>DDQ</sub> , AV <sub>DD</sub>	Supply voltage range		0.5 V to 3.6 V
V <sub>I</sub>	Input voltage range <sup>(2)(3)</sup>		–0.5 V to V <sub>DDQ</sub> + 0.5 V
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>		–0.5 V to V <sub>DDQ</sub> + 0.5 V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub>	±50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub>	±50 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>DDQ</sub>	±50 mA
I <sub>DDS</sub>	Continuous current to GND or V <sub>DDQ</sub>		±100 mA
T <sub>stg</sub>	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

(3) This value is limited to 3.6 V maximum.

### THERMAL CHARACTERISTICS

R <sub>θJA</sub> for TSSOP Package <sup>(1)</sup>	
Airflow	High K
0 ft/min (0 m/min)	94.4°C/W
150 ft/min (45.72 m/min)	82.8°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51.

**RECOMMENDED OPERATING CONDITIONS**

			MIN	NOM	MAX	UNIT	
Supply voltage	V <sub>DDQ</sub>	PC1600 – PC3200	2.3		2.7	V	
	AV <sub>DD</sub>		V <sub>DDQ</sub> – 0.12		2.7		
V <sub>IL</sub> Low-level input voltage	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$				V <sub>DDQ</sub> /2 – 0.18	V	
	PWRDWN		–0.3		0.7		
V <sub>IH</sub> High-level input voltage	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$		V <sub>DDQ</sub> /2 + 0.18			V	
	PWRDWN		1.7		V <sub>DDQ</sub> + 0.3		
DC input signal voltage <sup>(1)</sup>			–0.3		V <sub>DDQ</sub> + 0.3	V	
V <sub>ID</sub> Differential input signal voltage <sup>(2)</sup>	DC	CLK, FBIN	V <sub>DDQ</sub> = 2.3 V – 2.7 V		0.36	V <sub>DDQ</sub> + 0.6	V
			V <sub>DDQ</sub> = 2.425 V – 2.7 V		0.25	V <sub>DDQ</sub> + 0.6	
	AC	CLK, FBIN	V <sub>DDQ</sub> = 2.3 V – 2.7 V		0.7	V <sub>DDQ</sub> + 0.6	
			V <sub>DDQ</sub> = 2.425 V – 2.7 V		0.49	V <sub>DDQ</sub> + 0.6	
V <sub>IX</sub> Input differential pair cross voltage <sup>(3)(4)</sup>			V <sub>DDQ</sub> /2 – 0.2		V <sub>DDQ</sub> /2 + 0.2	V	
I <sub>OH</sub> High-level output current					–12	mA	
I <sub>OL</sub> Low-level output current					12	mA	
SR Input slew rate			1		4	V/ns	
T <sub>A</sub> Operating free-air temperature			–40		85	°C	

- (1) The unused inputs must be held high or low to prevent them from floating.
- (2) The dc input signal voltage specifies the allowable dc execution of the differential input.
- (3) The differential input signal voltage specifies the differential voltage |V<sub>TR</sub> – V<sub>CP</sub>| required for switching, where V<sub>TR</sub> is the true input level and V<sub>CP</sub> is the complementary input level.
- (4) The differential cross-point voltage is expected to track variations of V<sub>CC</sub> and is the voltage at which the differential signals must cross.

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub> Input voltage, all inputs	V <sub>DDQ</sub> = 2.3 V, I <sub>I</sub> = –18 mA			–1.2	V
V <sub>OH</sub> High-level output voltage	V <sub>DDQ</sub> = min to max, I <sub>OH</sub> = –1 mA	V <sub>DDQ</sub> – 0.1			V
	V <sub>DDQ</sub> = 2.3 V, I <sub>OH</sub> = –12 mA	1.7			
V <sub>OL</sub> Low-level output voltage	V <sub>DDQ</sub> = min to max, I <sub>OL</sub> = 1 mA			0.1	V
	V <sub>DDQ</sub> = 2.3 V, I <sub>OL</sub> = 12 mA			0.6	
V <sub>OD</sub> Output voltage swing <sup>(2)</sup>		1.1		V <sub>DDQ</sub> – 0.4	V
V <sub>OX</sub> Output differential cross-voltage <sup>(3)</sup>	Differential outputs are terminated with 120 Ω, C <sub>L</sub> = 14 pF (See Figure 3)	V <sub>DDQ</sub> /2 – 0.1	V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 + 0.1	V
I <sub>I</sub> Input current	V <sub>DDQ</sub> = 2.7 V, V <sub>I</sub> = 0 V to 2.7 V			±10	μA
I <sub>OZ</sub> High-impedance-state output current	V <sub>DDQ</sub> = 2.7 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND			±10	μA
I <sub>DDPD</sub> Power-down current on V <sub>DDQ</sub> + AV <sub>DD</sub>	CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I <sub>DD</sub> and AI <sub>DD</sub>	20		100	μA
AI <sub>DD</sub> Supply current on AV <sub>DD</sub>	f <sub>O</sub> = 170 MHz	6		8	mA
	f <sub>O</sub> = 200 MHz	8		10	
C <sub>I</sub> Input capacitance	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND	2	2.5	3.5	pF

- (1) All typical values are at a nominal V<sub>DDQ</sub>.
- (2) The differential output signal voltage specifies the differential voltage |V<sub>TR</sub> – V<sub>CP</sub>|, where V<sub>TR</sub> is the true output level and V<sub>CP</sub> is the complementary output level.
- (3) The differential cross-point voltage tracks variations of V<sub>DDQ</sub> and is the voltage at which the differential signals must cross.

**ELECTRICAL CHARACTERISTICS (continued)**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>DD</sub>	Dynamic current on V <sub>DDQ</sub>	Without load	f <sub>O</sub> = 170 MHz		65	80	mA
			f <sub>O</sub> = 200 MHz		75	90	
		Differential outputs terminated with 120 Ω, C <sub>L</sub> = 0 pF	f <sub>O</sub> = 170 MHz		110	140	
			f <sub>O</sub> = 200 MHz		120	150	
		Differential outputs terminated with 120 Ω, C <sub>L</sub> = 14 pF	f <sub>O</sub> = 170 MHz		130	160	
			f <sub>O</sub> = 200 MHz		140	170	
ΔC	Part-to-part input capacitance variation	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND				1	pF
C <sub>I(Δ)</sub>	Input capacitance difference between CLK and CLK, FBIN and FBIN	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND				0.25	pF

**TIMING REQUIREMENTS**

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		MIN	MAX	UNIT
f <sub>CLK</sub>	Operating clock frequency	60	220	MHz
	Application clock frequency	90	220	
Input clock duty cycle		40%	60%	
Stabilization time (PLL mode) <sup>(1)</sup>			10	μs
Stabilization time (bypass mode) <sup>(2)</sup>			30	ns

- (1) The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V<sub>DD</sub> must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.
- (2) A recovery time is required when the device goes from power-down mode into bypass mode (AV<sub>DD</sub> at GND).

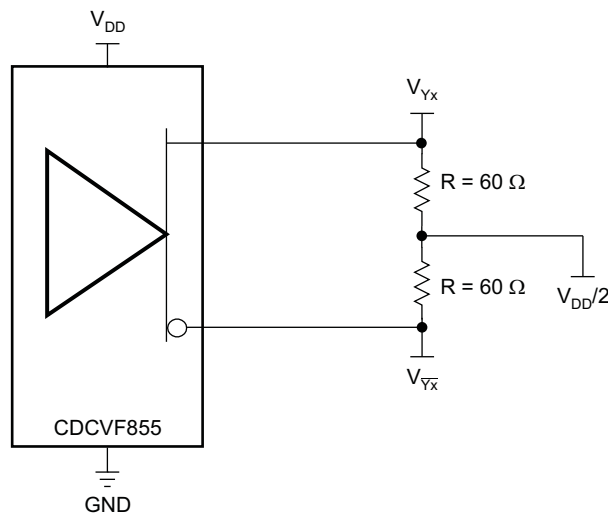
### SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}^{(1)}$	Low- to high-level propagation delay time	Test mode/CLK to any output		3.5		ns
$t_{PHL}^{(1)}$	High- to low-level propagation delay time	Test mode/CLK to any output		3.5		ns
$t_{jit(per)}^{(2)}$	Jitter (period), see Figure 7	100/133/167 MHz (PC1600/2100/2700)	-65		65	ps
		200 MHz (PC3200)	-30		30	
$t_{jit(cc)}^{(2)}$	Jitter (cycle-to-cycle), see Figure 4	100/133/167 MHz (PC1600/2100/2700)	-60		60	ps
		200 MHz (PC3200)	-40		40	
$t_{jit(hper)}^{(2)}$	Half-period jitter, see Figure 8	100/133/167 MHz (PC1600/2100/2700)	-100		100	ps
		200 MHz (PC3200)	-75		75	
$t_{srl(o)}$	Output clock slew rate, see Figure 9	Load: 120 $\Omega$ , 14 pF	1		2	V/ns
$t_{(o)}$	Static phase offset, see Figure 5	100/133/167/200 MHz	-50		50	ps
$t_{sk(o)}$	Output skew, see Figure 6	Load: 120 $\Omega$ , 14 pF; 100/133/167/200 MHz			40	ps

- (1) Refers to the transition of the noninverting output.
- (2) This parameter is assured by design but cannot be 100% production tested.

### PARAMETER MEASUREMENT INFORMATION



S0229-02

Figure 1. IBIS Model Output Load

PARAMETER MEASUREMENT INFORMATION (continued)

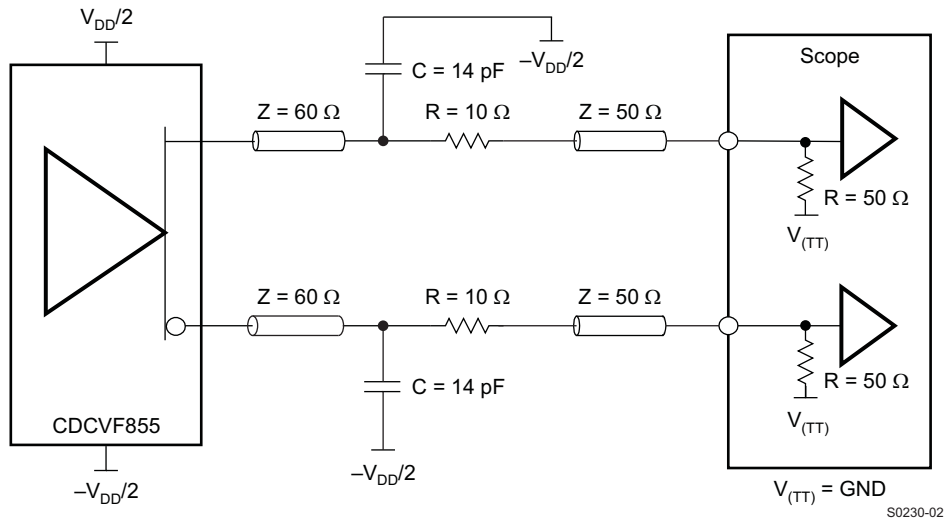


Figure 2. Output Load Test Circuit

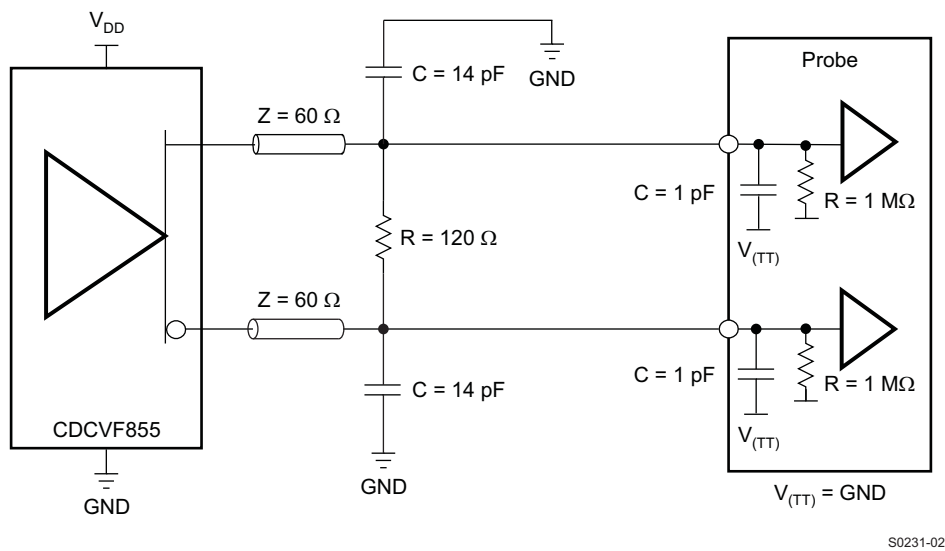
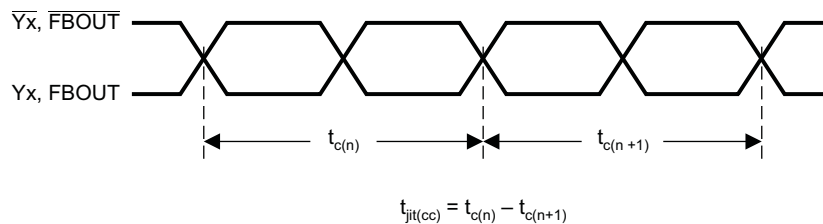


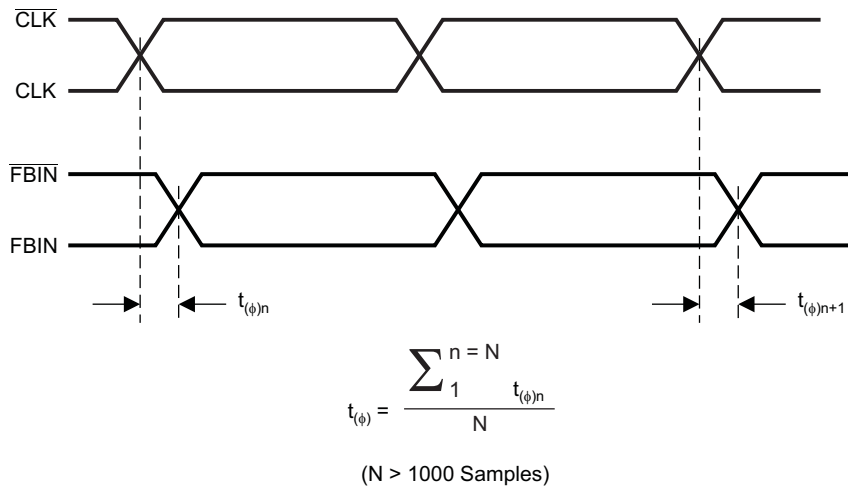
Figure 3. Output Load Test Circuit for Crossing Point



T0174-01

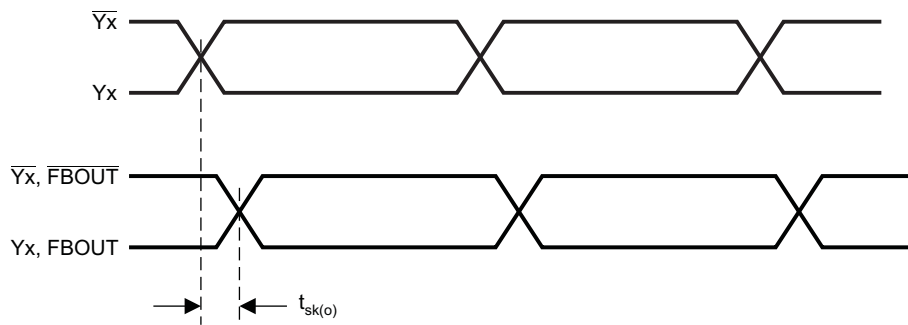
Figure 4. Cycle-to-Cycle Jitter

**PARAMETER MEASUREMENT INFORMATION (continued)**



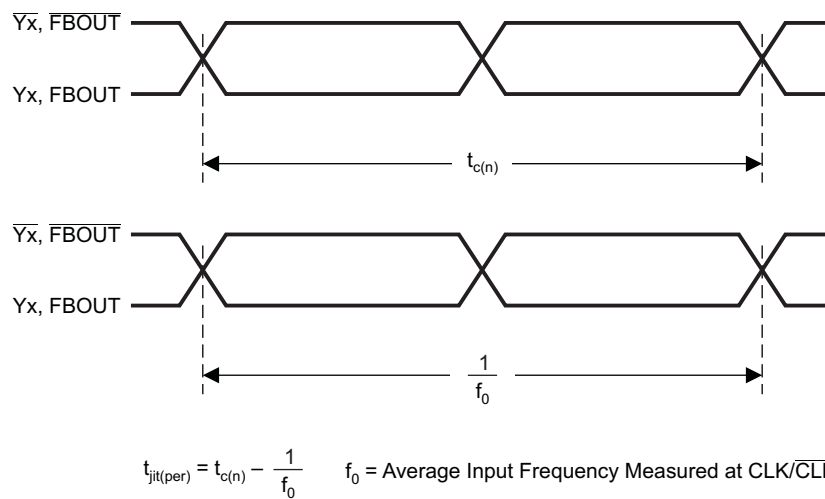
T0175-01

**Figure 5. Phase Offset**



T0176-01

**Figure 6. Output Skew**

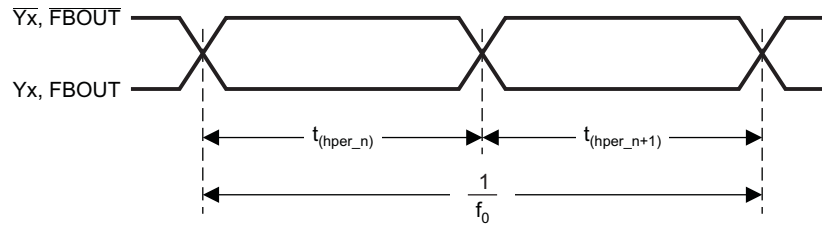


T0177-01

**Figure 7. Period Jitter**



PARAMETER MEASUREMENT INFORMATION (continued)

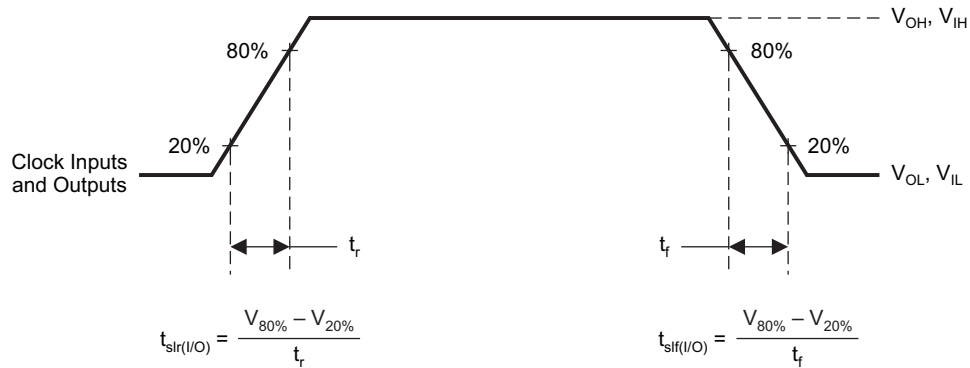


$$t_{jit(hper)} = t_{(hper\_n)} - \frac{1}{2 \times f_0}$$

n = Any Half Cycle  
f<sub>0</sub> = Average Input Frequency Measured at CLK/CLK

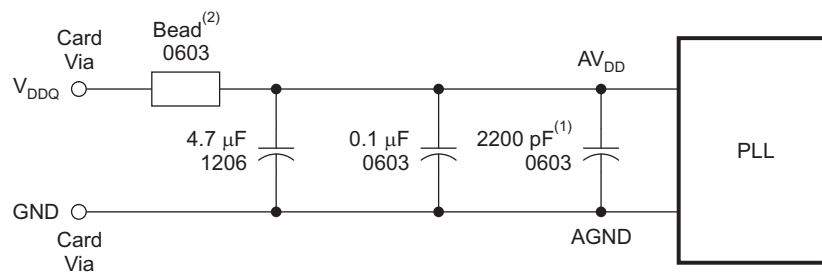
T0178-01

Figure 8. Half-Period Jitter



T0179-01

Figure 9. Input and Output Slew Rates



S0232-01

- (1) Place the 2200-pF capacitor close to the PLL.
- (2) Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

NOTE: Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).

Figure 10. Recommended AV<sub>DD</sub> Filtering

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDCVF855PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCVF855PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCVF855PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCVF855PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF855PWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF855PWR	TSSOP	PW	28	2000	346.0	346.0	33.0

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated